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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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Shan-Chyun Ku

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NORTH AMERICA INTELLECTUAL PROPERTY CORPORATION

P.O. BOX 506

MERRIFIELD, VA 22116

EXAMINER

DO, CHAT C

ART UNIT

PAPER NUMBER

2193

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

DETAILED ACTION

Drawings

1. Figures 1-5 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated as cited in under the description of the prior art section in original specification pages 1-9. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

3. Claim 1 is rejected under 35 U.S.C. 103(a) as being obvious over the admitted prior art in view of Sager et al. (U.S. 6,852,764).

Re claim 1, the admitted prior art discloses in Figures 1-5 a method for improving processing efficiency of pipeline architecture with a processor (e.g. col. 1 paragraph [0004] as pipeline architecture), the processor (e.g. Figure 1 and first three lines of

paragraph [0005]) having: a first functional unit for executing a calculation task (e.g. part 12 in Figure 1); a second functional unit for executing another calculation task (e.g. part 14 in Figure 1); and a control unit (e.g. part 16 in Figure 1) electrically connected to the first and the second functional units for generating a plurality of control signals to control the first and the second functional units (e.g. paragraphs [0005-0006] wherein the control unit 16 generates two control lines to functional units 12 and 14 for orderly and properly execute calculation task as seen in lines 7-15 in paragraph [0005]); the method comprising: (a)executing a first calculation task with the first functional unit or the second functional unit (e.g. part 12 in Figure 1, calculation F in Figure 3, paragraph [0008], and lines 5-6 in paragraph [0005]); (b)determining an executing time period of a second calculation task (e.g. part 12 in Figure 1, calculation D in Figure 3, and paragraph [0008]) with the control unit (e.g. part 16 in Figure 1 and paragraph [0008]) according to the functional unit executing the first calculation task (e.g. paragraph [0006] as the first functional unit executes in one cycle and the second functional unit executes in two cycles, and Figures 4-5 wherein the F, D, R...calculation tasks are executed sequentially), an executing time period of the first calculation task (e.g. last four lines in paragraph [0007], paragraphs [0009] and [0011], every task is executed in two cycles and the next calculation is waited for turn to be executed with stall cycle as necessary), (c)executing the second calculation task with the first functional unit (e.g. part 12 in Figure 1, calculation D in Figure 3, and paragraph [0008]) according to the executing time period of the second calculation task determined in step (b) (e.g. the controller unit 16 in Figure 1 is scheduled or controlled when to execute the task accordingly). The admitted prior art

fails to disclose the determination of an execution time also depend on whether the second calculation task depends upon a result of the first calculation task. However, Sager et al. disclose a pipeline architecture (e.g. abstract, col. 1 lines 33-63, and Figures 1-2) with the determination of an execution time also depend on whether the second calculation task depends upon a result of the first calculation task (e.g. col. 5 line 57 to col. 6 line 8 wherein the scheduler, for scheduling when to execute the instruction, will determine and verify the data dependencies from one instruction to another instruction before dispatch the next instruction in pipeline, and col. 5 line 50-58). Therefore, it would have been obvious to a person having ordinary skill in the art the time the invention is made to add a step of the determination of an execution time also depend on whether the second calculation task depends upon a result of the first calculation task as seen in Sager et al.'s invention into the admitted prior art's invention in pages 1-2 because it would enable to efficiency utilize the pipeline of calculation which leads to higher pipeline throughput (e.g. col. 1 lines 25-32, col. 1 lines 40-56, col. 2 lines 33-44, col. 3 lines 7-11, and col. 11 lines 54-68).

Allowable Subject Matter

4. Claim 6 is allowed.
5. Claims 2-5 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. The following is an examiner's statement of reasons for allowance:

The prior art of records fails to disclose or render an obviousness of a method for processing efficiency of pipeline architecture with a processor comprising: a control unit for controlling the first and the second functional units for executing first and second calculation task according to determination of executing time, wherein when the first calculation task is executed by the second functional unit within the first and the second time period and the second calculation task is executed by the first functional unit, if the second calculation task does not depend upon the result of the first calculation task, executing the second calculation task with the first functional unit within the second time period, if the second calculation task depends upon the result of the first calculation task, executing the second calculation task with the first functional unit within the third time period; when the first calculation task is executed by the first functional unit within the first time period and the second calculation task is also executed by the first functional unit, if the second calculation task does not depend upon the result of the first calculation task, executing the second calculation task with the first functional unit within the second time period, if the second calculation task depends upon the result of the first calculation task, executing the second calculation task with the first functional unit within the third time period; and when the first calculation task is executed by the first functional unit within the second time period and the second calculation task is also executed by the first functional unit, executing the second calculation task with the first functional unit within the third time period as seen in dependent claim 2 and independent claim 6.

The found closest prior arts are the admitted prior art and Sager et al. (U.S. 6,952,764). The admitted prior art in view of Sager et al. disclose a method for processing efficiency of pipeline architecture with a processor comprising: a control unit for controlling the first and the second functional units for executing first and second calculation task according to determination of executing time. However, the admitted prior art in view of Sager et al. fail to disclose the limitation of when the first calculation task is executed by the second functional unit within the first and the second time period and the second calculation task is executed by the first functional unit, if the second calculation task does not depend upon the result of the first calculation task, executing the second calculation task with the first functional unit within the second time period, if the second calculation task depends upon the result of the first calculation task, executing the second calculation task with the first functional unit within the third time period; when the first calculation task is executed by the first functional unit within the first time period and the second calculation task is also executed by the first functional unit, if the second calculation task does not depend upon the result of the first calculation task, executing the second calculation task with the first functional unit within the second time period, if the second calculation task depends upon the result of the first calculation task, executing the second calculation task with the first functional unit within the third time period; and when the first calculation task is executed by the first functional unit within the second time period and the second calculation task is also executed by the first functional unit, executing the second calculation task with the first functional unit within the third time period as seen in dependent claim 2 and independent claim 6.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.
- a. U.S. Patent No. 5,119,324 to Ahsan discloses an apparatus and method for performing arithmetic functions in a computer system.
 - b. U.S. Patent No. 4,935,849 to Miranker discloses a chaining and hazard apparatus and method.
 - c. U.S. Patent No. 6,965,906 to Dhablania discloses a converting negative floating-point numbers to integer notation without two's complement hardware.
 - d. U.S. Patent No. 7,007,059 to Mohammed et al. disclose a fast pipelined adder/subtractor using increment/decrement function with reduced register utilization.
 - e. U.S. Patent Publication No. 2004/0111455 to Skull discloses a hybrid arithmetic logic unit.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

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If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2193

July 21, 2006

A handwritten signature in black ink, appearing to be 'Chat C. Do', with a stylized, flowing script.